

IBM Docket No. PO920000107US1 Ser. No.:
09/841,505 Examiner M. Dimyan

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(A) AMENDMENT OF THE CLAIMS:

1 1. (Currently Amended) A logic synthesis method for reducing
2 the delay of a timing critical path in a circuit, comprising
3 the steps of:

4 (a) selecting a gate which is not an inverter in the
5 timing critical path [[,]];

6 (b) swapping said timing critical path to a pin of said
7 gate [[,]];

8

9 (c) replacing said gate with a functionally equivalent
10 tapered gate [[,]];

11

12 (d) performing a timing analysis of said circuit [[,]];
13 and

14 (e) if said timing analysis of said circuit
15 indicates improvement in a worst case delay through said
16 circuit [[,]];

17

18 (f) then retaining said tapered gate,
19 and

20 (g) if said timing analysis of said circuit indicates
21 no improvement in said worst case delay through said circuit
22 [[,]];

23

24 (h) then swapping said tapered gate back to said
25 selected gate for use in said circuit.

1 2. (Currently Amended) The logic synthesis method of claim 1
2 1 wherein

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3 said gate is selected from a gate library comprising a
4 set of non-tapered gates and a set of tapered gates, and
5 wherein in said gate library,
6 said non-tapered gates are characterized by a stack of
7 devices of the same width and said tapered gates are
8 characterized by a stack of devices of different widths.

1 3. (Currently Amended) The logic synthesis method of claim 1
2 1 wherein said gate is selected from a gate library
3 comprising a set of non-tapered gates and a set of tapered
4 gates,
5 and wherein each set in said gate library comprises one or
6 more of the following gates: NAND gates, NOR gates,
7 AND-OR-INVERT gates, and OR-AND-INVERT gates.

1 4. (Currently Amended) A logic synthesis method as in claim
2 3 1 whereby the delay through said tapered gate and the
3 delay through said non-tapered gate are compared.

1 [[6.]] 5. (Currently Amended) A logic synthesis method as in
2 claim 1 1 whereby a plurality of tapered gates exist for a
3 non-tapered gate, said plurality of tapered gates being
4 functionally equivalent to said non-tapered gate.

1 [[7.]] 6. (Currently Amended) A logic synthesis method as in
2 claim [[6]] 5, whereby the selection of said plurality of
3 tapered gates available for use in said circuit is swapped
4 into said circuit for comparison with a timing analysis of
5 the circuit.

1 [[8.]] 7. (Currently Amended) A logic synthesis method as in
2 claim [[7]] 6, whereby the delay through said plurality of

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3 tapered gates and the delay through said non-tapered gate
4 are compared.

1 [[9.]] 8. (Currently Amended) A logic synthesis method as in
2 claim [[8]] 7. whereby the gate of said plurality of gates
3 which yields the shortest delay is the one retained for said
4 circuit.